REMARKS

This response is intended as a full and complete response to the Office Action dated November 7, 2003. In view of the amendments and the following discussion, the Applicant believes that all claims are in allowable form.

REJECTIONS

35 U.S.C. §102

Claims 1-3

Claims 1-3 stand rejected as being anticipated by Japanese Patent No. 05224044A, published September 3, 1993 to Sumitomo Electric Company (Hereinafter *Sume*). In response, the Applicants have amended claim 1 to more clearly recite aspects of the invention.

Claim 1, as amended, recites limitations not taught or suggested by *Sume*. *Sume* teaches a waveguide formed in a substrate having a silicon surface. A feature (e.g., a ditch) is formed in the silicon surface. The feature is oxidized to form a lower clad layer. A core material is disposed in the feature, and optionally leveled. An upper clad layer is deposited over the core material. However, *Sume* does not teach or suggest forming an opening through a semiconductor layer to an underlying first insulating layer, as recited by claim 1.

Therefore, as the *Sume* does not teach or suggest the limitations of independent claim 1 and claims 2-3 that depend therefrom. Thus, the Applicants submit that claims 1-3 are patentable over *Sume*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

35 U.S.C. §103(a)

A. Claim 4

Claim 4 stands rejected as being unpatentable over *Sume* in view of United States Patent No. 6,553,170, issued April 22, 2002, to *Zhong* et al. (hereinafter *Zhong*). In response, the Applicants have amended claim 1 to more clearly recite aspects of the invention.

As discussed above, claim 1, from which claim 4 depends, recites limitations not taught or suggested by the *Sume*. *Zhong* teaches an optical waveguide having a dual layer top clad. *Zhong* teaches that the waveguide is formed on a substrate having a bottom cladding layer disposed thereon. Core material is disposed on the bottom cladding and subsequently covered by a dual layer top clad.

However, *Zhong* does not teach or suggest forming an opening through a semiconductor layer to an underlying first insulating layer, as recited by claim 1. Thus, the teachings of *Zhong* cannot be used to modify the steps utilized to fabricate the waveguide of *Sume* in a manner that would include forming an opening through a semiconductor layer to an underlying first insulating layer, as recited by claim 1.

Therefore, the combination of *Sume* and *Zhong* does not teach or suggest the limitations of independent claim 1, and claim 4 that depends therefrom. Thus, the Applicants submit that claim 4 is patentable over *Sume* in view of *Zhong*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

B. Claim 5

Claim 5 stands rejected as being unpatentable over *Sume* in view of United States Patent No. 6,282,358, issued August 28, 2001, to *Hornbeck* et al. (hereinafter *Hornbeck*). In response, the Applicants have amended claim 1 to more clearly recite aspects of the invention.

As discussed above, claim 1, from which claim 5 depends, recites limitations not taught or suggested by the *Sume*. *Hornbeck* teaches an optical waveguide having trench formed in a dielectric layer disposed on a substrate that is filled with an optically

transmissive material. A reflective material is disposed between the sidewalls of the trench and the transmissive material.

However, *Hornbeck* does not teach or suggest forming an opening through a semiconductor layer to an underlying first insulating layer, as recited by claim 1. Thus, the teachings of *Hornbeck* cannot be used to modify the steps utilized to fabricate the waveguide of *Sume* in a manner that would include forming an opening through a semiconductor layer to an underlying first insulating layer, as recited by claim 1.

Therefore, the combination of *Sume* and *Hornbeck* does not teach or suggest the limitations of independent claim 1, and claim 5 that depends therefrom. Thus, the Applicants submit that claim 5 is patentable over *Sume* in view of *Hornbeck*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

C. Claims 6-8

Claims 6-8 stands rejected as being unpatentable over *Sume* in view of the *Wolf* VLSI Publication (pages 191-192 and 219-220) (hereinafter *Wolf*), and in further view of United States Patent No. 5,877,065, issued March 2, 1999, to *Yallup* (hereinafter *Yallup*). In response, the Applicants have amended claims 6-8 to more clearly recite aspects of the invention.

As discussed above, *Sume* does not teach or suggest forming an opening through a semiconductor layer to an underlying first insulating layer, as recited by claim 6. *Wolf* teaches the use of silicon nitride films as a mask for the selective oxidation of silicon. However, *Wolf* does not teach or suggest forming an opening through a semiconductor layer to an underlying first insulating layer, as recited by claim 6. Thus, the teachings of *Wolf* cannot be used to modify the steps utilized to fabricate the waveguide of *Sume* in a manner that would include forming an opening through a semiconductor layer to an underlying first insulating layer, as recited by claim 6.

Yallup teaches a process for trench isolation in IC fabrication. *Yallup* describes etching a trench through a silicon layer of a silicon on insulator (SOI) substrate using a silicon dioxide mask. A dielectric is formed (preferably thermal grown) on the sidewalls of the trench. The interior region of the trench is filled with a thick polysilicon, which also

deposits over the mask. The polysilicon over the mask is removed by a blanket etching process to leave a portion of the etch polysilicon above the upper surface of the silicon layer. The mask is stripped by etching (for example, wet etching with HF), leaving the polysilicon extending above the upper surface of the silicon layer to a height "h". The structure is oxidized to form a field oxide layer that covers the polysilicon. The difference in oxidation rates between the polysilicon and surrounding silicon surface results in a generally planar field oxide surface.

Thus, *Yallup* does not teach or suggest processes related to forming an optical waveguide. As neither *Sume* nor *Wolf* teaches forming a waveguide on a SOI, a person would not look to *Yallup* to modify the waveguide fabrication techniques of *Sume* or *Wolf* in a manner that would yield the subject matter of claim 6.

Therefore, the combination of *Sume*, *Wolf* and *Yallup* does not teach or suggest the limitations of independent claim 6, and claim 7-8 that depend therefrom. Thus, the Applicants submit that claims 6-8 are patentable over *Sume* in view of *Wolf* and in further view of *Yallup*. Accordingly, the Applicants respectfully request the rejection be withdrawn.

NEW CLAIMS

New claims 9-20 have been added to more clearly recite aspects of the invention. The Applicant believes new claims are fully supported by the specification, and accordingly, request allowance of these claims.

CONCLUSION

Thus, the Applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and swift passage to issue are earnestly solicited.

If the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Keith Taboada at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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Signature

KEITH TABOADA
Printed Name of Person Signing

12/24/2003
Date of signature